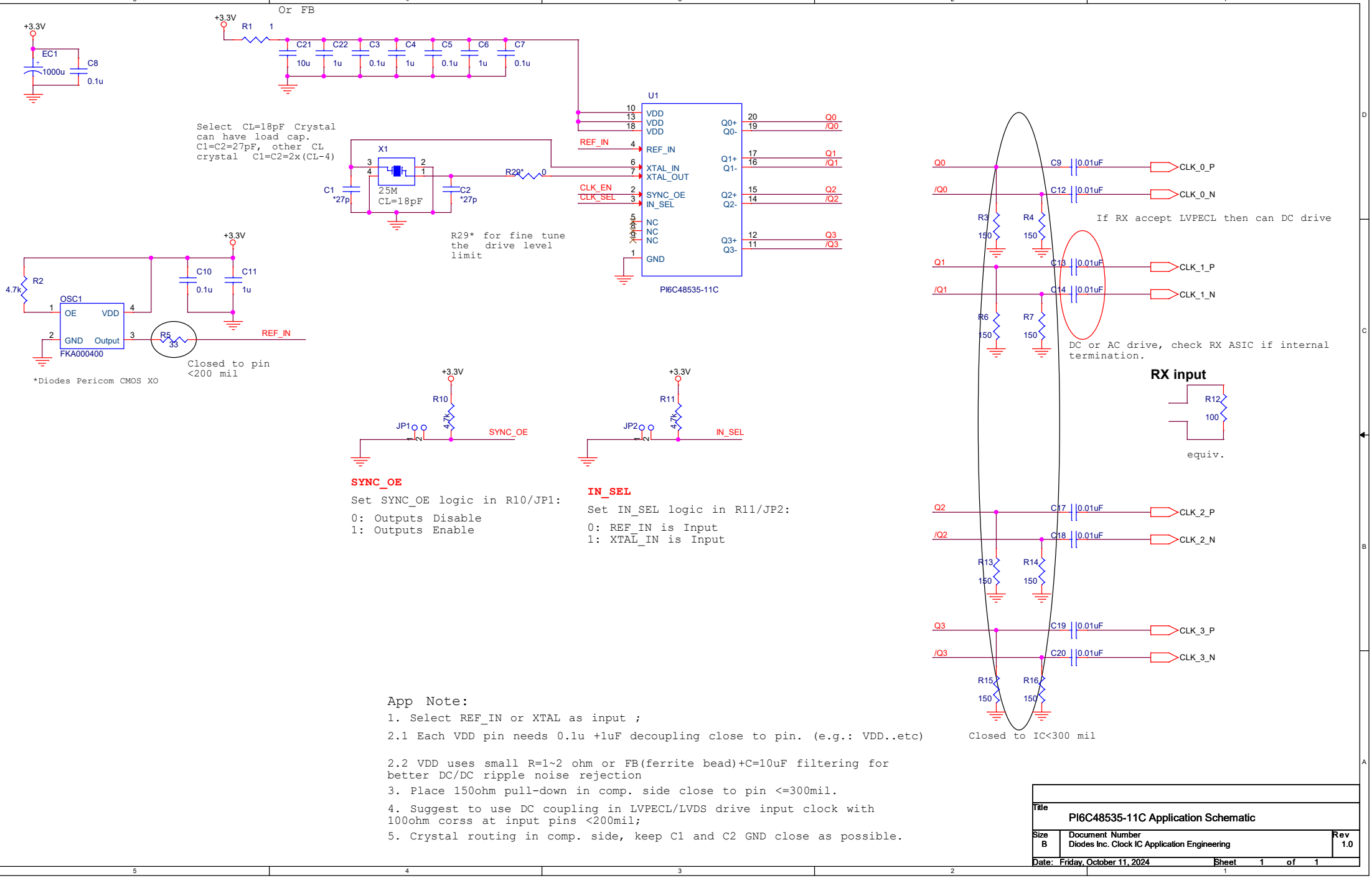


## App Note:

1. Select REF_IN or XTAL as input ;
2. 1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD..etc)
2. 2 VDD uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Place 150ohm pull-down in comp. side close to pin <=300mil.
4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;
5. Crystal routing in comp. side, keep C1 and C2 GND close as possible.

| | | |
|---|---|---|
| Title: PI6C48535-11C Application Schematic | | |
| Size: B | Document Number: Diodes Inc. Clock IC Application Engineering | Rev: 1.0 |
| Date: Friday, October 11, 2024 | Sheet 1 of 1 | |